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1 Estimation of standby leakage power in CMOS circuits considering accurate modeling of transistor stacks
Zhanping Chen, Mark Johnson, Liqiong Wei, Kaushik Roy
August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design**
Full text available: pdf(736.39 KB) Additional Information: full citation, abstract, references, citings, index terms

Low supply voltage requires the device threshold to be reduced in order to maintain performance. Due to the exponential relationship between leakage current and threshold voltage in the weak inversion region, leakage power can no longer be ignored. In this paper we present a technique to accurately estimate leakage power by accurately modeling the leakage current in transistor stacks. The standby leakage current model has been verified by IISPICE. We demonstrate that the dependence of leaka ...

2 Managing leakage power: Distributed sleep transistor network for power reduction
Changbo Long, Lei He
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(162.79 KB) Additional Information: full citation, abstract, references, citings, index terms

Sleep transistors are effective to reduce dynamic and leakage power. The cluster-based design was proposed to reduce the sleep transistor area by clustering gates to minimize the simultaneous switching current per cluster and then inserting a sleep transistor per cluster. In the paper, we propose a novel distributed sleep transistor network (DSTN), and show that DSTN is *intrinsically* better than the cluster-based design in terms of the sleep transistor area and circuit performance. We rev ...

3 A comparison of dual-rail pass transistor logic families in 1.5V, 0.18µm CMOS technology for low power applications
G. D. Gristede, Wei Hwang
March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**
Full text available: pdf(465.08 KB) Additional Information: full citation, abstract, references, index terms

In this paper the results of an experimental comparison of popular pass-transistor logic families in 1.5V, 0.18µm CMOS technology using advanced CAD tools for circuit tuning and simulation are presented. The logic families were compared using an experimental setup designed to clarify the strengths and weaknesses of each family in a relative fashion and

evaluate their individual performances under identical operating conditions. An automatic circuit tuner was used to help ensure that the ...

4 Leakage analysis and optimization: Post-layout leakage power minimization based on distributed sleep transistor insertion
Pietro Babighian, Luca Benini, Alberto Macii, Enrico Macii
August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**
Full text available: pdf(267.93 KB) Additional Information: full citation, abstract, references, index terms

This paper introduces a new approach to sub-threshold leakage power reduction in CMOS circuits. Our technique is based on automatic insertion of sleep transistors for cutting sub-threshold current when CMOS gates are in stand-by mode. Area and speed overhead caused by sleep transistor insertion are tightly controlled thanks to: (i) a post-layout incremental modification step that inserts sleep transistors in an existing row-based layout; (ii) an innovative algorithm that selects the subset of ce ...

Keywords: leakage power, sleep transistor, sub-threshold current

5 Mixed-Vth (MVT) CMOS circuit design methodology for low power applications
Liqiong Wei, Zhanping Chen, Kaushik Roy, Yibin Ye, Vivek De
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(236.18 KB) Additional Information: full citation, references, citings, index terms

6 Energy efficient memory systems: Drowsy instruction caches: leakage power reduction using dynamic voltage scaling and cache sub-bank prediction
Nam Sung Kim, Krisztián Flautner, David Blaauw, Trevor Mudge
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.10 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

On-chip caches represent a sizeable fraction of the total power consumption of microprocessors. Although large caches can significantly improve performance, they have the potential to increase power consumption. As feature sizes shrink, the dominant component of this power loss will be leakage. In our previous work we have shown how the drowsy circuit---a simple, state-preserving, low-leakage circuit that relies on voltage scaling for leakage reduction---can be used to reduce the total energy co ...

7 Tools and architectures for power minimization: Reducing leakage energy in FPGAs using region-constrained placement
A. Gayasen, Y. Tsai, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, T. Tuan
February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**
Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, references, citings, index terms

FPGAs are being increasingly used in a wide variety of applications. While power optimization has been only of secondary importance in many FPGA applications, growing importance of leakage in FPGAs designed in 90nm and below makes it imperative to treat power optimization as a first class citizen. In this paper, we propose a leakage-saving technique for FPGAs that involves dividing the FPGA fabric into small regions and switching on/off the power supply to each region using a sleep transistor in ...

Keywords: FPGA, leakage power, region-constrained placement

8 Design and optimization of low voltage high performance dual threshold CMOS circuits
Liqiong Wei, Zhanping Chen, Mark Johnson, Kaushik Roy, Vivek De
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**
Full text available: pdf(454.66 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Reduction in leakage power has become an important concern in low voltage, low power and high performance applications. In this paper, we use dual threshold technique to reduce leakage power by assigning high threshold voltage to some transistors in non-critical paths, and using low-threshold transistors in critical paths. In order to achieve the best leakage power saving under target performance constraints, an algorithm is presented for selecting and assigning an optimal high threshold vo ...

Keywords: MPEG4, codec, design automatian, flip-flops, level converters, low power, placement, synthesis, voltage scaling

9 Dynamic fine-grain leakage reduction using leakage-biased bitlines
Seongmoo Heo, Kenneth Barr, Mark Hampton, Krste Asanović
May 2002 **ACM SIGARCH Computer Architecture News**, Volume 30 Issue 2
Full text available: pdf(1.06 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Leakage power is dominated by critical paths, and hence dynamic deactivation of fast transistors can yield large savings. We introduce metrics for comparing fine-grain dynamic deactivation techniques that include the effects of deactivation energy and startup latencies, as well as long-term leakage current. We present a new circuit-level technique for leakage current reduction, leakage-biased bitlines, that has low deactivation energy and fast wakeup times. We show how this technique can be appl ...

Keywords: Dynamic Leakage Reduction

10 A survey of power management techniques in mobile computing operating systems
Gregory F. Welch
October 1995 **ACM SIGOPS Operating Systems Review**, Volume 29 Issue 4
Full text available: pdf(763.75 KB) Additional Information: full citation, abstract, index terms

Many factors have contributed to the birth and continued growth of mobile computing, including recent advances in hardware and communications technology. With this new paradigm however come new challenges in computer operating systems development. These challenges include heretofore relatively unusual items such as frequent network disconnections, communications bandwidth limitations, resource restrictions, and power limitations. It is the last of these challenges that we shall explore in this p ...

11 Architectures: Evaluation of low-leakage design techniques for field programmable gate arrays
Arifur Rahman, Vijay Polavarapuv
February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

Full text available: pdf(448.42 KB) Additional Information: full citation, abstract, references, index terms

In this paper we evaluate the trade-offs between various low-leakage design techniques for field programmable gate arrays (FGPAs) in deep sub-micron technologies. Since multiplexers are widely used in FPGAs for implementing look up tables (LUTs) and connection and routing switches, several low-leakage implementations of pass transistor based multiplexers and routing switches are proposed and their design trade-offs are presented based on transistor-level simulation, physical design, and impact o ...

Keywords: FPGA, leakage power, multiplexer

12 An improved pass transistor synthesis method for low power, high speed CMOS circuits

Tudor Vinereanu, Sverre Lidholm

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

Full text available: pdf(155.99 KB) Additional Information: full citation, abstract, references, index terms

A synthesis method for generating hybrid pass gate circuits is presented. These circuits combine features from both complementary CMOS and pass gates architectures. The simulation results using a 0.7 &mgr;m technology show that circuits synthesized according to the proposed method may achieve significant improvements in terms of area, power and delay over traditional full swing pass transistor logic and complementary CMOS.

13 Energy aware design: Optimizing pipelines for power and performance

Viji Srinivasan, David Brooks, Michael Gschwind, Pradip Bose, Victor Zyuban, Philip N. Strenski, Philip G. Emma

November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.24 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

During the concept phase and definition of next generation high-end processors, power and performance will need to be weighted appropriately to deliver competitive cost/performance. It is not enough to adopt a CPI-centric view alone in early-stage definition studies. One of the fundamental issues confronting the architect at this stage is the choice of pipeline depth and target frequency. In this paper we present an optimization methodology that starts with an analytical power-performance model ...

14 Low power caches: Understanding and minimizing ground bounce during mode transition of power gating structures

Suhwan Kim, Stephen V. Kosonocky, Daniel R. Knebel

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(139.98 KB) Additional Information: full citation, abstract, references, index terms

We introduce and analyze the ground bounce due to power mode transition in power gating structures. To reduce the ground bounce, we propose novel power gating structures in which sleep transistors are turned on in a non-uniform stepwise manner. Our power gating structures reduce the magnitude of peak current and voltage glitches in the power distribution network as well as the minimum time required to stabilize power and ground. Experimental simulation results with PowerSpice fixtured in a packa ...

Keywords: clock gating, ground bounce, inductive noise, power gating, system-on-a-chip (SOC) design, wake-up latency

15 Poster Session 1: Low-leakage asymmetric-cell SRAM

Navid Azizi, Andreas Moshovos, Farid N. Najm

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available: pdf(137.96 KB) Additional Information: full citation, abstract, references, citings, index terms

We introduce a novel family of asymmetric dual-Vt SRAM cell designs that reduce leakage power in caches while maintaining low access latency. Our designs exploit the strong bias towards zero at the bit level exhibited by the memory value stream of ordinary programs. Compared to conventional symmetric high-performance cells, our cells offer significant leakage reduction in the zero state and in some cases also in the one state albeit to a lesser extend. A novel sense-amplifier, in coor ...

Keywords: SRAM, dual-Vt, low-leakage, low-power

16 Optimizing CMOS Circuits for Low Power Using Transistor Reordering

Enric Musoll, Jordi Cortadella

March 1996 **Proceedings of the 1996 European conference on Design and Test**

Full text available: pdf(749.81 KB) Publisher Site Additional Information: full citation, abstract

This paper addresses the optimization of a circuit for low power using transistor reordering. The optimization algorithm relies on a stochastic model of a static CMOS gate that includes the power of internal nodes of the gate. This power-consumption model depends on the switching activity and the equilibrium probabilities of the inputs of the gate. The model allows an exploration of the different configurations of a gate that are obtained by reordering its transistors. Thus, the best configurati ...

Keywords: low-power design, power modeling, transistor reordering, combinational synthesis

17 Silicon trends and limits for advanced microprocessors

Mark Bohr

March 1998 **Communications of the ACM**, Volume 41 Issue 3

Full text available: pdf(221.08 KB) Additional Information: full citation, references, citings, index terms

18 Synchroscalar: A Multiple Clock Domain, Power-Aware, Tile-Based Embedded Processor

March 2004 **ACM SIGARCH Computer Architecture News , Proceedings of the 31st annual international symposium on Computer architecture**, Volume 32 Issue 2

Full text available: pdf(286.10 KB) Additional Information: full citation, abstract

We present Synchroscalar, a tile-based architecture forembedded processing that is designed to provide the flexibilityof DSPs while approaching the power efficiency ofASICs. We achieve this goal by providing high parallelismand voltage scaling while minimizing control and communicationcosts. Specifically, Synchroscalar uses columnsof processor tiles organized into statically-assignedfrequency-voltage domains to minimize power consumption.Furthermore, while columns use SIMD control to minimizeove ...

19 An Efficient Algorithm for Low Power Pass Transistor Logic Synthesis

Rupesh S. Shelar, Sachin S. Sapatnekar
January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**
Full text available: pdf(233.23 KB) Publisher Site Additional Information: full citation, abstract

In this paper, we address the problem of power dissipation minimization in combinational circuits implemented using pass transistor logic (PTL). We transform the problem of power reduction in PTL circuits to that of BDD decomposition and solve the latter using the max-flow min-cut technique. We use transistor level power estimates to guide the BDD decomposition algorithm. We present the results obtained by running our algorithm on a set of MCNC benchmark circuits, and show on an average of 47% p ...

Keywords: Logic Synthesis, Pass Transistor Logic, Low Power

20 Static power driven voltage scaling and delay driven buffer sizing in mixed swing QuadRail for sub-1V I/O swings
R. Krishnamurthy, I. Lys, L. Carley
August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design**
Full text available: pdf(226.83 KB) Additional Information: full citation, references, citings, index terms

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